ADVANCED RESEARCH & INNOVATIONS
International Journal of Advanced Research & Innovations
Volume 15, Issue-2
September, 2025, P71
ISSN: 2319-9253

International Conference on Emerging Trends in Engineering, Technology & Management (ICETM-2025)
Conducted by *Viswam Engineering College (UGC—Autonomous Institution)* held on 11th & 12th, April- 2025

A PERFORMANCE ANALYSIS OF EXCLUSIVE OR GATE USING DYNAMIC CMOS GATE LOGIC

T Jayasimha[1], Associate Professor,
Department of ECE, Viswam Engineering College, Madanapalle, India
Email: Jayasimha412@gmail.com
T Hussaini[2], Associate Professor,
Department of ECE, Viswam Engineering College, Madanapalle, India
Email: hussainik@gmail.com

ABSTRACT: Dynamic Pass transistor logic used in the digital circuits to reduce the transistor count, it arises node to get discharged properly, even with the pull-down network OFF during evaluation. An EXOR gate is implemented with the dynamic logic where clock signal is directly accessed the stacking effect circuitry, and it is altered to implement a new design of static CMOS dynamic logic with lower leakage power than older designs that used in nano meter technology the Micro wind 10nm technology used to validate the logic design methods and implementation of pass transistor logic with low input logic An EXOR gate is implemented with the dynamic logic where clock signal is directly accessed the stacking effect circuitry, and it is altered to implement a new design of static CMOS dynamic logic with lower leakage power than older designs that used in nano meter technology the Micro wind 10nm technology used to validate the logic design methods and implementation of pass transistor logic with low input logic.

Keywords*: Dynamic CMOS logic, EX-OR gate, Micro-Wind*

1. INTRODUCTION:

The high performance and low power consumption has become important in today's VLSI circuit design. The exponential growth of portable electronic devices like laptops, multimedia and cellular device, research efforts in the field of low power VLSI systems have increased. Now a day's low power consumption along with minimum delay and area requirements is one of important design consider for IC designers. There are three major sources of power consumption in VLSI circuits:

1) Switching power due to charge and discharge of capacitances.
2) Short circuit power due to current flow from power supply to ground with simultaneous function of p-network and n-networks.
3) Static power due to leakage currents.

The need for higher performance has used a Dynamic circuit where conventional static CMOS circuits may not meet the low critical path delay.

Hybrid CMOS logic styles have a higher design freedom to the desired performance. Hybrid full adder has higher speed, less power consumption and higher performance. Full adders are fundamental in various circuits which is used for performing arithmetic operations such as addition, subtraction, multiplication, address calculation, comparator and MAC etc. Enhancing the performance of the full adders can significantly affect the whole system performance.

When developing a complete adder, there are two logical approaches: static style and dynamic style. While dynamic full adders are faster and occasionally more compact than static ones, static full adders are more

Volume 15, Issue-2
September, 2025, P71
ISSN: 2319-9253

dependable, straightforward, and require less power. Techniques for achieving power consumption at the expense of performance are provided by recent technological scaling and the usage of several logic families. ower, speed, and durability are so important to cutting edge designs that they must be considered at every stage of the design process. There are two logic approaches for designing a full adder first is static style and second is dynamic style. Static full adder are more reliable, simpler and low power than dynamic ones but dynamic full adder are faster and sometimes more compact than static full adder. transistor width has loads down a previous stage of logic, for a particular current drive, Favors dynamic over static logic. This is critical since the high speed ensures that a speed advantage can be gained without loading down the cell greatly.

2. NOISE TOLERANT DYNAMIC TECHNIQUES

Noise is a phenomenon which causes our output to change from normal value to an abnormal value. Noise can be measured in terms of noise margin. Noise margin may be defined as the ability of a circuit to withstand noise. Gate internal and external noise are some classification of noise in dynamic logic circuit1. For improvement of noise immunity in dynamic CMOS logic gates a large number of techniques have been developed. These are listed as under

1. Dynamic feed through logic;
2. Diode footed domino;
3. Precharging internal nodes;
4. Raising source voltage;
5. Using keeper.

Dynamic Logic EX-OR gates.

Dynamic pass transistor logic implementation along with pass transistor logic where For the SPICE simulations to be accurate, we took great pains to optimize the process file for all ranges of operation. This optimization was accomplished using dynamic pass transistor logic with that software, we measured isolated bulk transistors and extracted the optimized process file. The transistors were made using a 0. 18- m process with a 0. 3 - V. the resulting process files were used in SPICE circuit

Dynamic logic is a clocked logic family which means that every single logic has a clock signal present. When the clock signal turns low, node N0 goes high, causing the output of the gate to go low. The mechanism for the gate output to go low once it has been driven high. The operating period of the cell when its input and output are low is called the recharge phase. The next phase, when the clock is high, is called as evaluate phase. The evaluate phase is the functional operating phase in dynamic cells, with the recharge phase enabling the evaluate phase to occur.

The application of the clock signal ensures that the critical path in dynamic cells only traverses through cells in the evaluate phase. Since the dynamic cell only switches from a low to a high direction, there is no need for the inputs to drive any pull-up PMOS transistors. The lack of a PMOS transistor means that the effective

As mentioned earlier, traditional scaling analyses emphasize the importance of trying to maintain a constant to preserve the switching speed. As we try to scale below 1 V,it becomes tempting to raise this ratio slightly. Unfortunately, this is not the only source of delay penalty when we raise the ratio. In single-transistor pass-gate logic, a drop is lost across the device when it tries to pull the output high. This signal degradation subsequently slows the pulldown of the output buffer and causes leakage because the pullup is not fully off. Since DTMOS circuits potentially lower the on-state threshold voltage to zero or below, pass-gate logic may benefit further from such designs.

ADVANCED RESEARCH & INNOVATIONS
International Journal of Advanced Research & Innovations
Volume 15, Issue-2
September, 2025, P71
ISSN: 2319-9253

In dynamic logic cells, the evaluate phase is the functional functioning phase, and the recharge phase makes it possible for the evaluate to phase to take place. The critical path in dynamic pass transistor logic cells that develops high efficiency on the adder and other application that passes through cells in the evaluate phase tanks to the clock signal's application. No pullup PMOS transistors need to be driven by the inputs because the dynamic logic cell only shifts from a low to a high direction. Because there is not a PMOS transistor, the effective transistor width loads down a prior logic stage, dynamic logic over static logic for a given current drive.

In this method of noise immunity is applicable as it gives more noise immunity in addition to low power. It is shown in Figure 5(b). As the clk is kept higher these transistor Mr is turned ons, discharged the output node. This phase known as reset phase. Evaluation phase comes into play when the clock goes low. Initially there is false logic evaluation occurs and there is no path between transistor Mq and pull down network as all inputs to NMOS are reset to low in this period. After finishing that the inputs obtain their correct logic value and hence S evaluates to correct logic level. If the input combination applied is such that the pull down network is ON then contention takes place between PMOS and pull down network. In the evaluation period although it has performance advantage FTL results in lesser noise margins and direct and non-zero nominal low output voltage. Thus, to remove this problem modified feed through logic technique was introduced. Here an additional PMOS transistor is used to decrease charge sharing between internal node and dynamic node.

3. RESULTS AND DISCUSSION:

The results and discission on dynamic pass transistor logic during pre-charge phase and evaluation phase logic in micro wind tool and layout design implementation

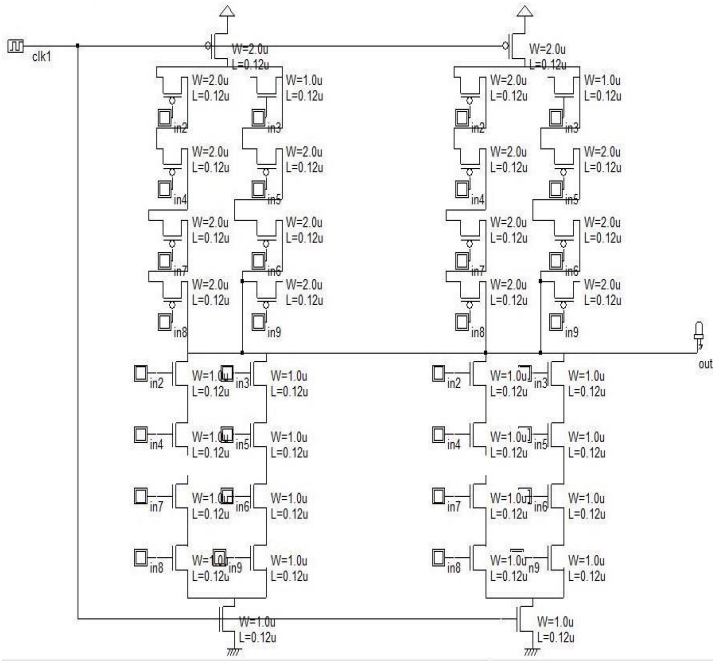

Figure 1 Layout Representation of EX-OR gate

ADVANCED RESEARCH & INNOVATIONS
International Journal of Advanced Research & Innovations
Volume 15, Issue-2
September, 2025, P71
ISSN: 2319-9253

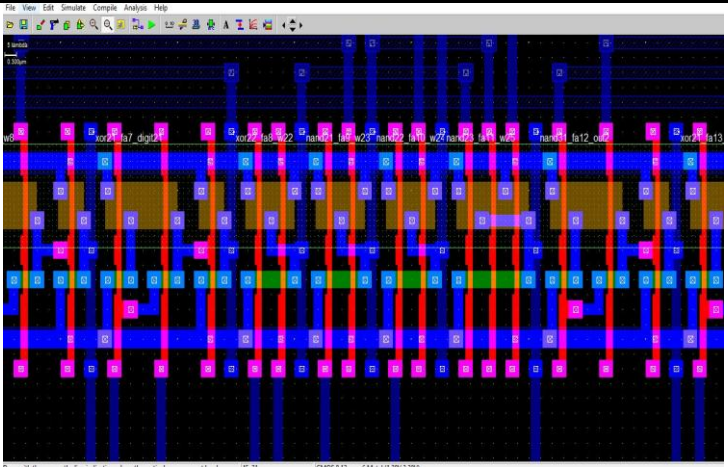

Figure2 Layout Representation of EX-OR gate

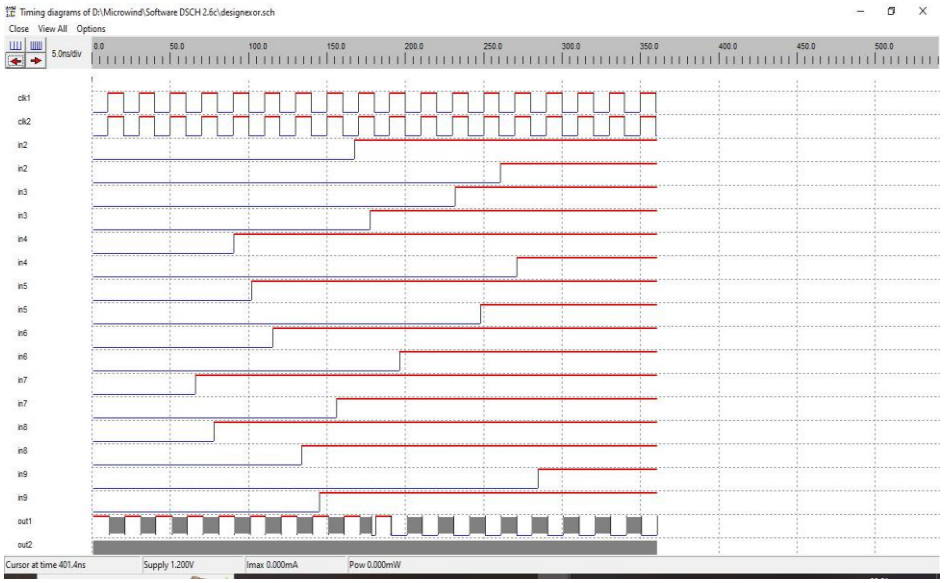

Figure 3 Timing Representation of Dynamic EX-OR gate

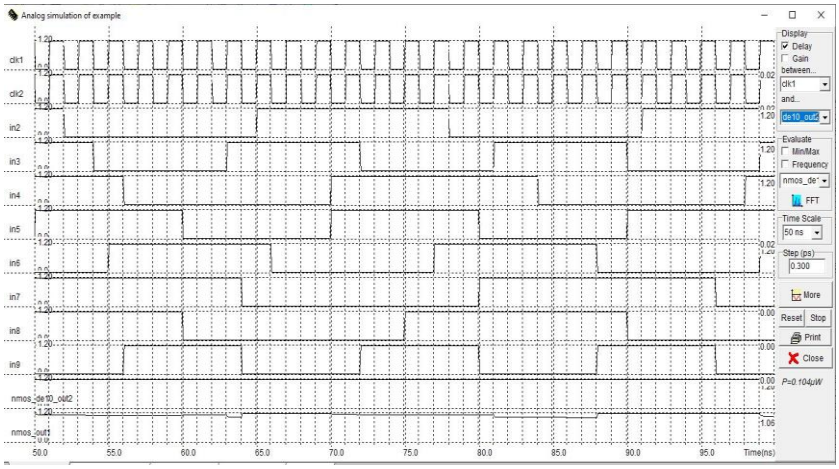

Figure 4 Timing Representation of Dynamic EX-OR gate

Volume 15, Issue-2
September, 2025, P71
ISSN: 2319-9253

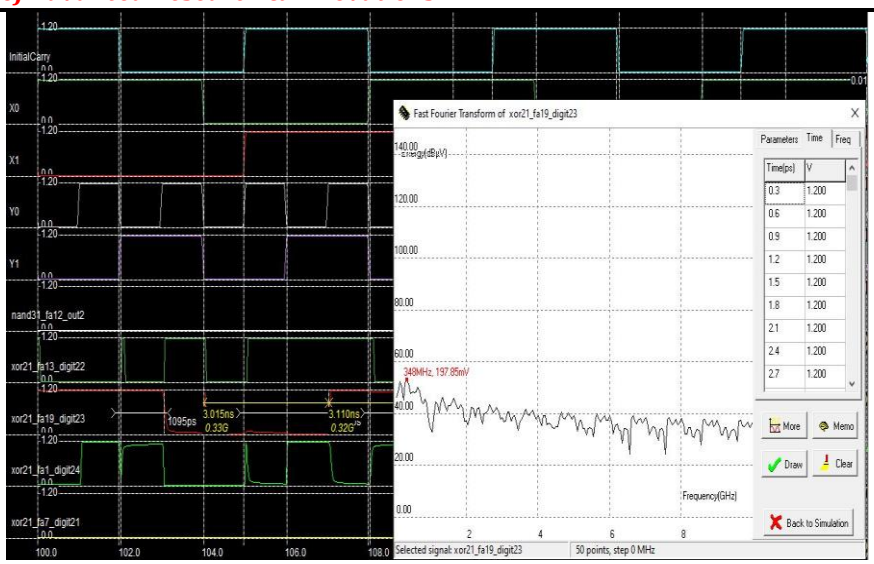

Figure 5 Noise immunity Eye diagram of dynamic CMOS Logic

4. CONCLUSION AND FUTURE WORK

Different noise tolerant identification has been discussed using dynamic CMOS and pass transistor logic used is very helpful in providing good noise immunity and gives lesser power consumption in addition to lesser immunity Thus, to remove this problem modified feed through logic technique was introduced. Here an additional PMOS transistor is used to decrease charge sharing between internal node and dynamic node. Techniques like internal node Precharging puts forward the problem of dc power consumption. It is effectively used for only specific types of logics. Diode Footed Domino is mostly used for high fan-in circuits and is a leakage tolerant and high-performance technique. It gave better results than conditional keeper technique which can see in the table and graph given below.

REFERENCES

[1] B. Parhami, Computer Arithmetic, Algorithm and Hardware Design, *Oxford University Press*, New York, pp. 91-119, 2000.

[2] Stephen Brown and Zvonko Vranesic, Fundamentals of Digital Logic with VHDL Design. *2nd Ed. McGraw-Hill Higher Education,* USA.ISBN: 0072499389, 2005.

[3] B. Goll and H. Zimmermann, "A comparator with reduced delay time in 65-nm CMOS for supply voltages down to 0.65," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 56, no. 11, pp. 810–814, Nov. 2009.

[4] Jinhui Wang, Wuchen Wu, Ligang Hou, Shuqin Geng and Wang Zhang, Xiaohong Peng, "Using Charge Self-compensation Dynamic Full-adder with Multiple Supply and Dual Thresho

[5] M. S. Abadir and H. K. Reghabati, "Functional test generation for digital circuits described using binary decision diagram," *IEEE Trans. Comput.*, vol. C-35, pp. 375–379, Apr. 1986.

[6] S. B. Akers, "Binary decision diagrams," *IEEE Trans. Comput.*, vol.C-27, pp. 509–516, June 1978.

[7] W. Al-assadi, A. P. Jayasumana, and Y. K. Malaiya, "Pass-transistor logic design," *Int. J. Electron.*, vol. 70, pp. 739–749, 1991.

[8] P. Ashar, S. Devadas, and K. Keutzer, "Testability properties of multilevel logic networks derived from binary decision diagrams," in *Proc.Santa Cruz Conf. Advanced Res. VLSI*, Mar. 1991, pp. 35–54.

[9] C. L. Berman, "Ordered binary decision diagrams and circuit structures, "in *Proc. IEEE Int. Conf. Computer Design: VLSI in Computers*, 1989, pp. 392–395.

[10] K. Bartlett, R. K. Brayton, G. Hachtel, R. Jacoby, R. Rudell, A. Sangiovanni-Vincentelli, and A. Wang, "Multilevel logic minimization using implicit don't cares," *IEEE Trans. Computer-Aided Design*, vol.7, pp. 723–740, 1988.

[11] J. R. Burch, E. M. Clarke, K. L. McMillan, and D. L. Dill, "Sequential circuit verification using symbolic model checking," in *Proc. 27thIEEE/ACM Design Automat. Conf.*, 1990, pp. 46–51.

[12] S. Chakravarty, "A testable multiplexer realization of CMOS combination circuits," in *Proc. 1989 IEEE Int. Test Conf.*, pp. 509–518.

[13] S. Chakravarty, "A characterization of binary decision diagrams," *IEEETrans. Comput.*, vol. 42, pp. 129–136, Feb. 1993.

[14] T. S. Cheung and K. Asada, "Regenerative pass-transistor logic: A circuit technique for high speed digital design," *IEICE Trans. Electron.*,vol. E79-C, no. 9, pp. 1274–1284, Sept. 1996.

[15] A. Jaekel, "Synthesis of multilevel pass transistor logic networks," Ph.D. dissertation, University of Windsor, 1995.

[16] G. A. Jullien, W. C. Miller, R. Grondin, L. Del Pup, S. Bizzan, and D.Zhang, "Dynamic computational blocks for bit-level systolic arrays," *IEEE J. Solid-State Circuits*, vol. 29, no. 1, pp. 14–22, 1994.

[17] G. A. Jullien, N. M. Wigley, and J. Reilly, "VLSI implementations of number theoretic concepts with applications in signal processing," invited chapter in *Handbook of Statistics*, N. K Bose and C. R. Rao Eds. Elsevier Science Publishers, 1993, vol. 10, ch. 13, pp. 535–576.

[18] Y. Kanie, Y. Kubota, S. Toyoyama, Y. Iwase, and S. Tsuchimoto, "4-2 compressor with complementary pass-transistor logic," *IEICE Trans.Electron.*, vol. E77-C, no. 4, pp. 647–649, Apr. 1994