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A PERFORMANCE ANALYSIS OF PSEUDO NMOS LOGIC FOR PROCESS PARAMETERS

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ABSTRACT: In the paper, we study linear operators Wide fan-in logic gates when implemented in static complementary CMOS logic consume a significant area overhead, consume a large power consumption, and have a large propagation delay.The circuit design issues of this family are discussed. Also, it is compared with the conventional CMOS logic from the circuit design issues of this family are discussed. Also, it is compared with the conventional CMOS logic from the points of view of the area, the average propagation delay, the average power consumption, and the logic swing using a proper figure of merit. The effects of technology scaling and process variations on this family are investigated.

Keywords: area, propagation delay, pseudo-PMOS logic, wide fan-in.

1. INTRODUCTION

In this section, the pseudo-NMOS logic is verified by simulation adopting the 45 nm CMOS technology with VDD= 0.8 V . Assume minimum-sized devices and a frequency of operation equal to 500 MHz. As a compromise between the enhancement of the logic swing and the degradation in the high-to-low propagation delay with increasing Vthn, MN is chosen with a threshold voltage equal to 0.7 V and biased by VB= VDD. In evaluating the low-to-high or the high-to-low propagation delays, the 50% criterion is adopted. The worst-case scenarios are also adopted the average propagation delays, respectively, versus the number of the inputs, n, for the conventional and pseudo-NMOS logic families. The low-to-high propagation delay according to the pseudo-NMOS logic is found to be smaller than that of the conventional one for all values of n. The superiority in performance of the pseudo-PMOS logic during the low-to-high transition is attributed to the need to charge all the internal capacitances of the pull-down network in the conventional CMOS stack.

Although the contention current of MN slows down the charging of CL in the pseudo-PMOS logic, it does not affect the performance considerably. The average energy-delay products according to the proposed and conventional schemes in Joule-Seconds. Conventional CMOS proposed scheme.

2. PSEUDO NMOS LOGIC DESIGN

A Pseudo-PMOS Logic for Realizing Wide Fan-in Two important notes are in order here. The first one is that the pseudo-PMOS logic family can be used in realizing any logic circuit with series or parallel connections in the PUNs or PDNs. In this case, the PUN is the same as that of the conventional

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CMOS logic. The pseudo-PMOS logic is obviously not suitable for realizing logic circuits containing serially connected PMOS transistors in their PUNs as it requires a significant area overhead. The second note is that the quantitative analysis of the next section can be applied equally well to the pseudo-NMOS logic after substituting the acronyms associated with the NMOS devices by those of the PMOS ones and vice versa Conventionally, the VLSI digital systems are performed with the conventional logic in Boolean space. Recently, the Dynamic logic is widely used in high performance microprocessors and is attractive for high speed circuits as compared to static logic. Dynamic circuits use fifty percent of transistor check concerning integral static circuits. Domino reason networks are high power effective & co-operatively quicker. Domino method of reasoning is on a very basic level a dynamic basis network sought after by a static inverter & capacitor as a stack.

Dynamic rationale circuit yield is put away in the capacitor, it is associated next beyond the static inverter. The task of domino rationale circuit controlled by TVL is used to design the digital circuits because it offers reduced chip-area, low interconnect complexity, reduced digits needed to represent a number, low power dissipation, *etc.* over the conventional logic. Thus, the main drawback of this logic is very high static power consumption as there exists a direct path between Vdd and ground through the PMOS transistor. In order to make low output voltage as small as possible, the pMOS device should be sized much smaller than the nMOS pull-down devices. Also, to increase the speed particularly when driving many other gates the pMOS transistor size has to be made larger. Therefore there is always a trade-off between the parameters noise margin, static power dissipation and propagation delay.

Complementary metal oxide semiconductor (CMOS) technology requires multi-threshold transistors. However, the multi-threshold voltage CMOS transistors are acquired by biasing the bulk terminal. Using the bulk biasing technique to design the TVL circuits is time consuming and complex task. Hence, the researchers looked for alternative technologies such as quantum-dot FETs, reversible logics, single-electron transistors and Out of them, using technology is optimistic way to develop the TVL digital logic circuits because the multi-threshold can be obtained by changing the diameter of CNT. Moreover, the technology offers 10 times more energy efficiency compared to CMOS technology while designing the circuits. Each of the proposed circuits consists of only two inputs A and B and more than two outputs depending on the design. The main design objectives for these circuits are low power consumption and higher speed at low supply voltage.

So as to enhance exhibitions a higher drive charge equivalently scaled the transistor edge potential level. Because of high spillage charge, cross-talk, commotion, input clamor & current sharing builds the profound sub-micron clamor level. The sub edge spillage current generously expands edge voltage scaling results. Increments of spillage of the assessment transistors exponentially because of scale down, while expanded crosstalk the commotion at the contribution of the advancement transistors may increments.

3. SIMULATION RESULTS

A compromise between the enhancement of the logic swing and the degradation in the high-to-low propagation delay with increasing Vthn, MN is chosen with a threshold voltage equal to 0.7 v and biased by VB= VDD. In evaluating the low-to-high or the high-to-low propagation delays, the 50% criterion is adopted. The worst-case scenarios are also adopted.

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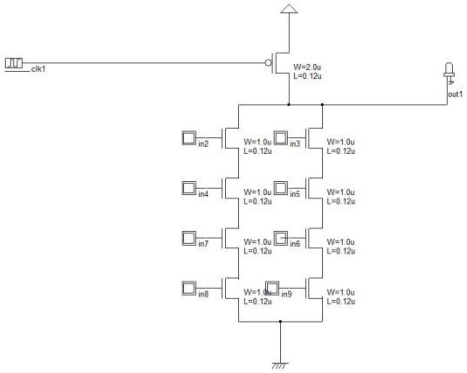

Figure:1 Pseudo NMOS logic

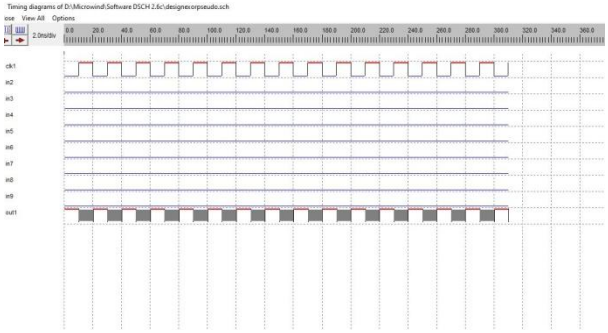

Figure:2 Pseudo NMOS exor logic

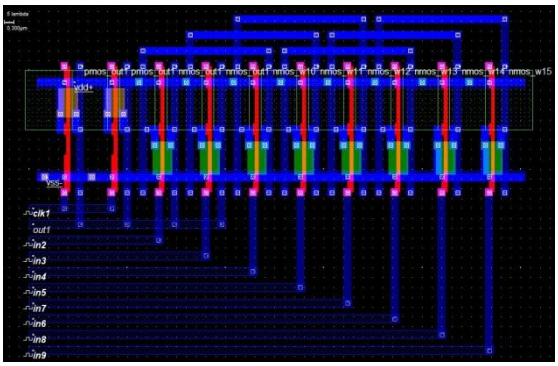

Figure: 3 Pseudo NMOS exor layout logic

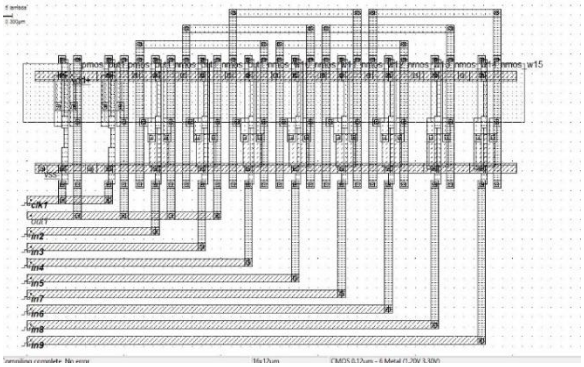

Figure: 4 Pseudo NMOS exor layout logic

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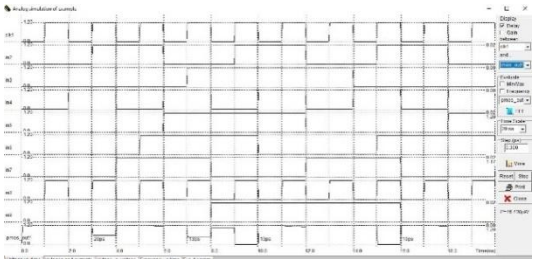

Figure: 5 Pseudo NMOS exor layout logic timing daigram

4. CONCLUSION

The performance analysis of Pseudo-NMOS logic reveals that while it offers advantages in terms of reduced transistor count, simplified design, and faster switching speed compared to CMOS logic, its performance is highly sensitive to process parameters such as threshold voltage (Vth), channel length, and supply voltage variations. The static power dissipation due to the always-on pull-up PMOS transistor remains a major drawback, especially as technology scales down.

Optimization of the pull-up to pull-down ratio is essential to balance power consumption and noise margin. Overall, Pseudo-NMOS logic provides a favorable trade-off between speed and area for specific high-performance applications, but careful consideration of process variations is necessary to maintain reliability and energy efficiency in modern VLSI design.

REFERENCES

1. K. Martin, Digital Integrated Circuit Design, Oxford University Press, New York, 2000.
2. M. M. Khellah and M. I. Elmasry, "Use of Charge Sharing to Reduce Energy Consumption in Wide Fan-In Gates," Proceedings of the IEEE International Symposium on Circuits and Systems, 31 May -3 Jun. 1998.
3. S. C. Prasad and K. Roy, "Transistor Reordering for Power Minimization under Delay Constraint," ACM Transactions on Design Automation Elect. Syst., Vol. 1, No. 2, Pages: 280 -300, Apr. 1996.
4. E. Musoll and J. Cortadella, "Optimizing CMOS Circuits for Low Power Using Transistor Reordering," Proceedings of European Design and Test Conference, Pages: 219 -223, 1996.
5. C. Tan and J. Allen, "Minimization of Power in VLSI Circuits Using Transistor Sizing, Input Ordering, and Statistical Power Estimation," Proceedings of International Workshop Low-Power Design, Pages: 75 – 80, 1994.
6. W. H. Chiu and H. R. Lin, "A Conditional Isolation Technique for Low-Energy and High-Performance Wide Domino Gates," IEEE Region 10 Conference, 30 Oct. -2 Nov. 2007.
7. H. Mostafa, M. Anis, and M. Elmasry, "Novel Timing Yield Improvement Circuits for High-Performance Low-Power Wide Fan-In Dynamic OR Gates," IEEE Transactions on Circuits and Systems I: Regular Papers, Vol. 58, Issue: 8, Pages:1785– 1797, Aug. 2011.234567800.511.522.533.5x 10-24The number of the inputs,
8. K. Mohanram and N. A. Touba, "Lowering Power Consumption in Concurrent Checkers via Input References Références

9. A. A. George and A. R. Sankar, "Current Comparison Based High Speed Domino Circuits," National Conference on Science, Engineering, and Technology (NCSET), Vol. 4, Issue: 6, Pages: 102 –105, 2016.
10. F. Moradi, D. T. Wisland, H. Mahmoodi, and T. V. Cao, "High Speed and Leakage-Tolerant Domino Circuits for High Fan-in Applications in 70nm CMOS Technology," Proceedings of the 7thInternational Caribbean Conference on Devices, Circuits, and Systems, Mexico, 28 -30 Apr., 2008.
11. K. Rajasri, M. Manikandan, A. J. Dhanaseely, and M. Nishanthi, "Low Leakage High Speed Domino Circuit For Wide Fan-in Equality Comparator," International Journal of Advanced Research in Electronics and Communication Engineering (IJARECE), Vol. 4, Issue: 3, Mar. 2015.
12. Anamika and G. N. Chiranjeevi, "Low Power Wide Fan In Domino OR Logics," International Journal of Current Engineering and Scientific Research, (IJCESR), Vol. 3, Issue: 7, Pages: 39 –43, 2016.
13. X. Kavousianos and D. Nikolos, "Novel Single and Double Output TSC Berger Code Checkers," Proceedings of VLSI Test Symposium, Pages: 348 –353, 1998.
14. C. Metra, M. Favalli, and B. Ricco, "Tree Checkers for Applications with Low Power-Delay Requirements," Proceedings of International Symposium on Defect and Fault Tolerance VLSI Systems, Pages: 213 –220, 1996.
15. B. Razavi, Design of Analog CMOS Integrated Circuits, SecondEdition, McGraw-Hill, New York, 2016.
16. H. Shichman and D. Hodges, "Modeling and Simulation of Insulated-Gate Field-Effect Transistor Switching Circuit," IEEE Journal of Solid-State Circuits, Vol. sc-13, No. 3, Pages: 285 - 289, Sep. 1968.
17. A. S. Sedra and K. C. Smith, Microelectronic Circuits, Seventh Edition, Oxford University Press.